CY7C460A/CY7C462A
CY7C464A/CY7C466A

Asynchronous, Cascadable 8K/16K/32K/64K x9 FIFOs

Features

- **High-speed, low-power, first-in first-out (FIFO) memories**
- **8K x 9 FIFO (CY7C460A)**
- **16K x 9 FIFO (CY7C462A)**
- **32K x 9 FIFO (CY7C464A)**
- **64K x 9 FIFO (CY7C466A)**
- **10-ns access times, 20-ns read/write cycle times**
- **High-speed 50-MHz read/write independent of depth/width**
- **Low operating power**
  - **— I_{CC}= 60 mA**
  - **— I_{SB} =8 mA**
- **Asynchronous read/write**
- **Empty and Full flags**
- **Half Full flag (in standalone mode)**
- **Retransmit (in standalone mode)**
- **TTL-compatible**
- **Width and Depth Expansion Capability**
- **5V ± 10% supply**
- **PLCC, LCC, 300-mil and 600-mil DIP packaging**
- **Three-state outputs**
- **Pin compatible density upgrade to CY7C42X/46X family**
- **Pin compatible and functionally equivalent to IDT7205, IDT7206, IDT7207, IDT7208**

Functional Description

The CY7C460A, CY7C462A, CY7C464A, and CY7C466A are respectively, 8K, 16K, 32K, and 64K words by 9-bit wide first-in first-out (FIFO) memories. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another by passing tokens.

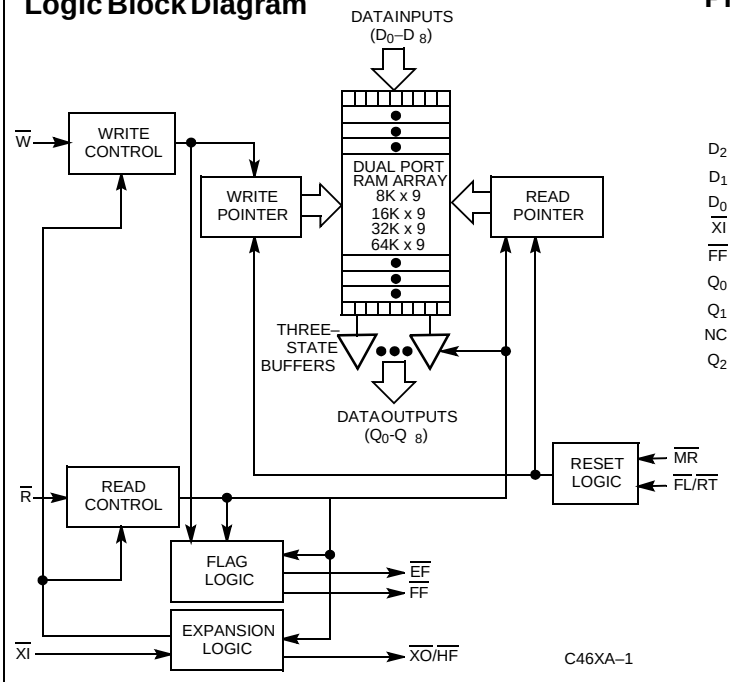
The read and write operations may be asynchronous; each can occur at a rate of up to 50 MHz. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone (single device) and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the Retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data.

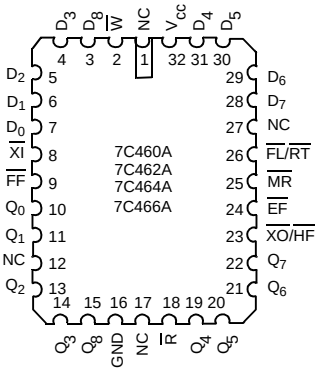
The CY7C460A, CY7C462A, CY7C464A, and CY7C466A are fabricated using Cypress's advanced 0.5µ RAM3 CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout and the use of guard rings.

Logic Block Diagram



Pin Configurations

PLCC/LCC Top View



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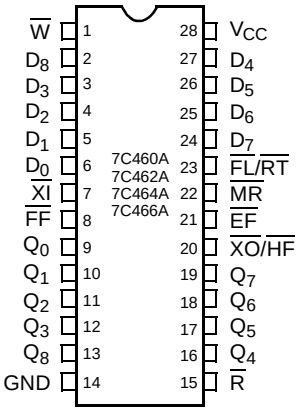
DIP Top View



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Selection Guide

	7C460A-10 7C462A-10 7C464A-10 7C466A-10	7C460A-15 7C462A-15 7C464A-15 7C466A-15	7C460A-25 7C462A-25 7C464A-25 7C466A-25
Frequency (MHz)	50	40	28.5
Maximum Access Time (ns)	10	15	25

Maximum Ratings [1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Military[2]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

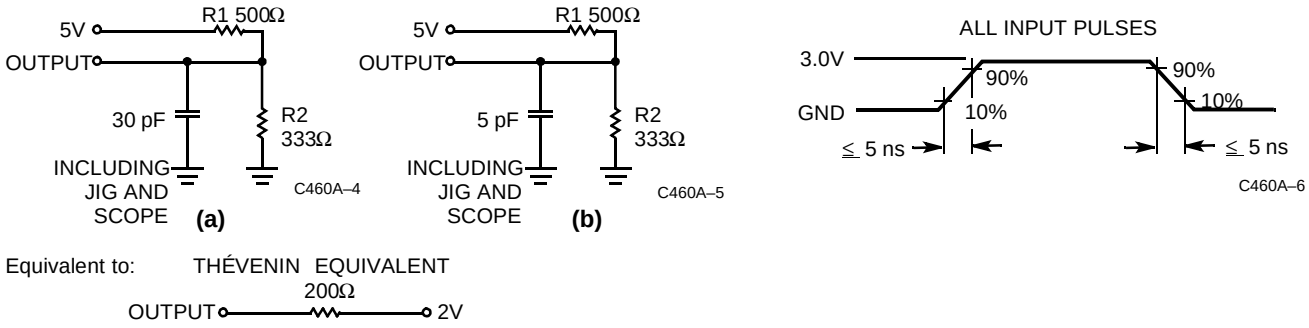
Parameter	Description	Test Conditions	7C460A/462A/464A/466A (-10,-15,-25)		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Freq. = 20 MHz		60	mA
I_{SB}	Standby Current	All Inputs = V_{IH} min.		8	mA

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	10	pF
C_{OUT}	Output Capacitance		12	pF

Notes:
1. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C460A-10 7C462A-10 7C464A-10 7C466A-10		7C460A-15 7C462A-15 7C464A-15 7C466A-15		7C460A-25 7C462A-25 7C464A-25 7C466A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	20		25		35		ns
t_A	Access Time		10		15		25	ns
t_{RR}	Read Recovery Time	10		10		10		ns
t_{PR}	Read Pulse Width	10		15		25		ns
t_{LZR}	Read LOW to Low Z	3		3		3		ns
t_{DVR}[7]	Data Valid After Read HIGH	3		3		3		ns
t_{HZR}[7]	Read HIGH to High Z		15		15		18	ns
t_{WC}	Write Cycle Time	20		25		35		ns
t_{PW}	Write Pulse Width	10		15		25		ns
t_{HWZ}	Write HIGH to Low Z	5		5		5		ns
t_{WR}	Write Recovery Time	10		10		10		ns
t_{SD}	Data Set-Up Time	9		9		9		ns
t_{HD}	Data Hold Time	0		0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	20		25		35		ns
t_{PMR}	$\overline{MR}$ Pulse Width	10		15		25		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	10		15		25		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	10		15		25		ns
t_{RTC}	Retransmit Cycle Time	20		25		35		ns
t_{PRT}	Retransmit Pulse Width	10		15		25		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		20		25		35	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		20		25		35	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		20		25		35	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		10		15		25	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		10		15		25	ns

Notes:

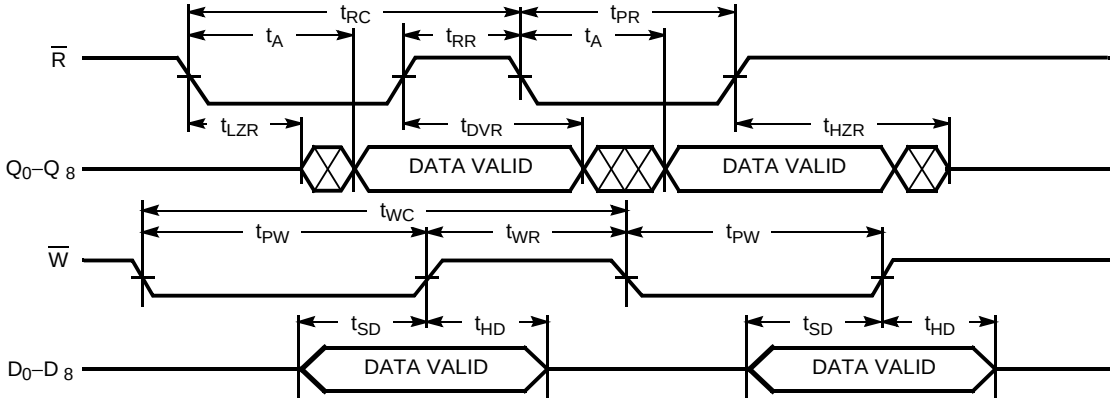
6. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Loads, unless otherwise specified.
7. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Loads.

Switching Characteristics Over the Operating Range[3, 6] (continued)

Parameter	Description	7C460A-10 7C462A-10 7C464A-10 7C466A-10		7C460A-15 7C462A-15 7C464A-15 7C466A-15		7C460A-25 7C462A-25 7C464A-25 7C466A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		10		15		25	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		10		15		25	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		10		15		35	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		10		15		35	ns
t_{RAE}	Effective Read from Write HIGH		10		15		25	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	10		15		25		ns
t_{WAF}	Effective Write from Read HIGH		10		15		25	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	10		15		25		ns
t_{XOL}	Expansion Out LOW Delay from Clock		10		15		25	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		10		15		25	ns

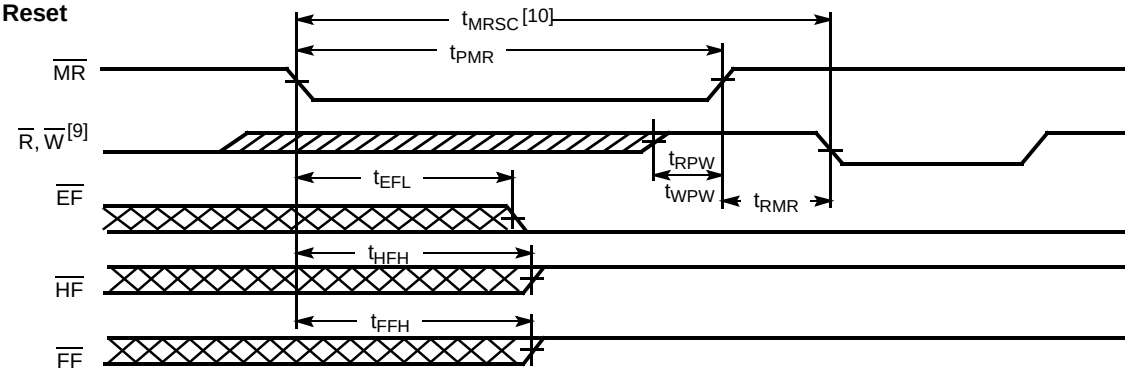
Switching Waveforms[7]

Asynchronous Read and Write



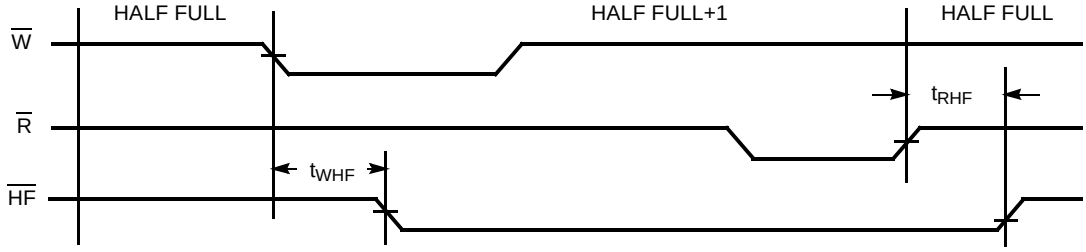
C460A–7

Master Reset



C460A–8

Half Full Flag



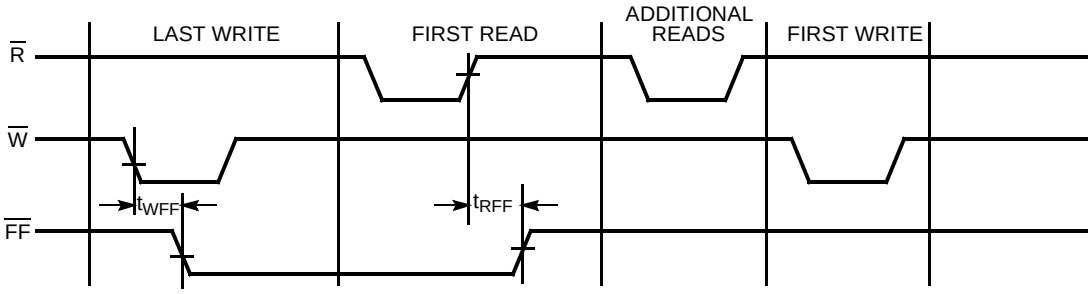
C460A–9

Notes:

8. A HIGH-to-LOW transition of either the write or read strobe causes a HIGH-to-LOW transition of the responding flag. Correspondingly, a LOW-to-HIGH strobe transition causes a LOW-to-HIGH flag transition.
9. W and R = V_{IH} around the rising edge of MR.
10. $t_{MSRC} = t_{PMR} + t_{RMR}$

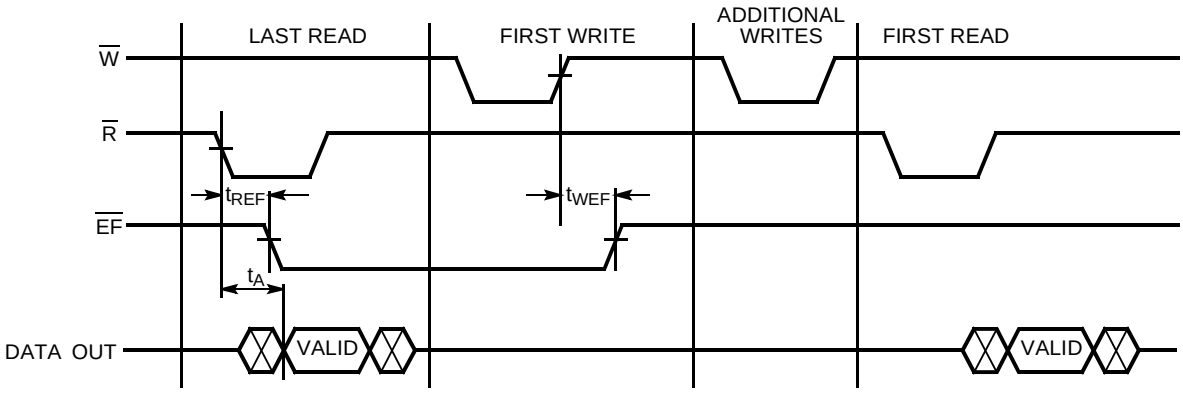
Switching Waveforms[7] (continued)

Last Write to First Read Full Flag



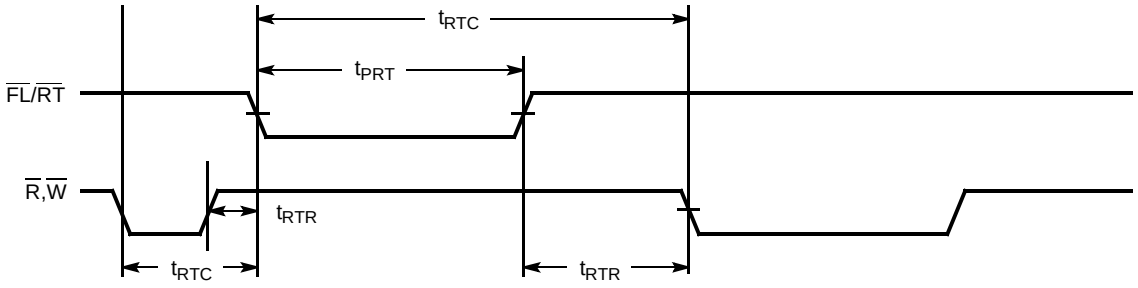
C460A–10

Last READ to First WRITE Empty Flag



C460A–11

Retransmit[11,12]



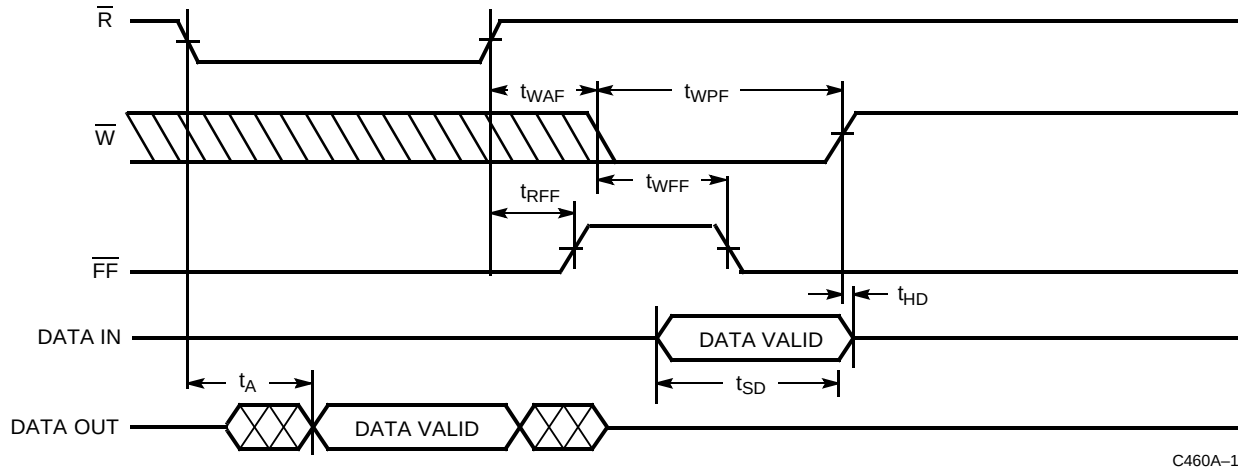
C460A–12

Notes:

11. $t_{RTC} = t_{PRT} + t_{RTR}$.
12. EF, HF, and FF may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}, except for the CY7C46x-20 (Military), whose flags will be valid after t_{RTC} + 10 ns.

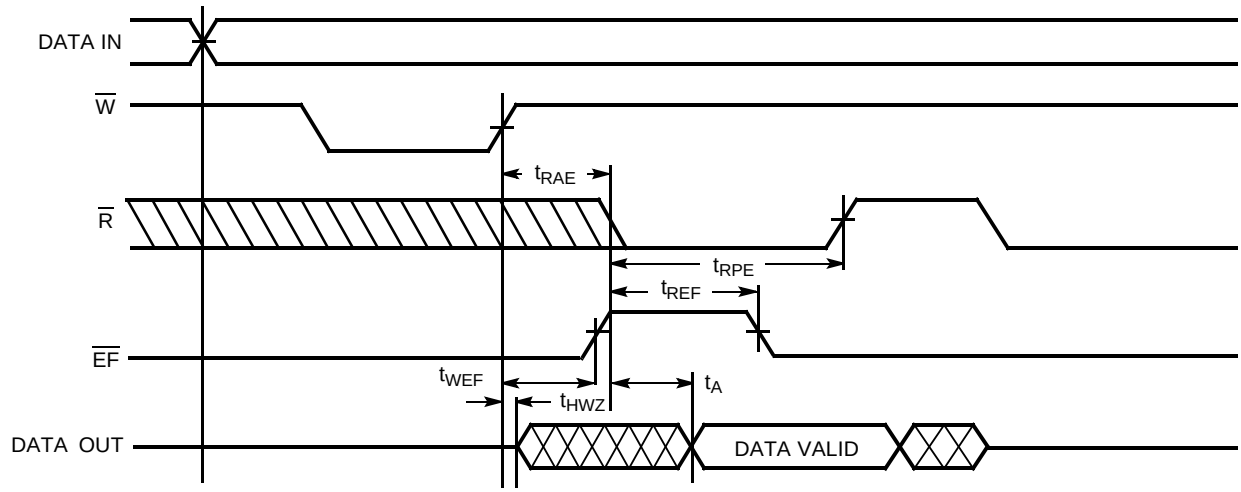
Switching Waveforms[7] (continued)

Full Flag and Write Data Flow-Through Mode



C460A–1

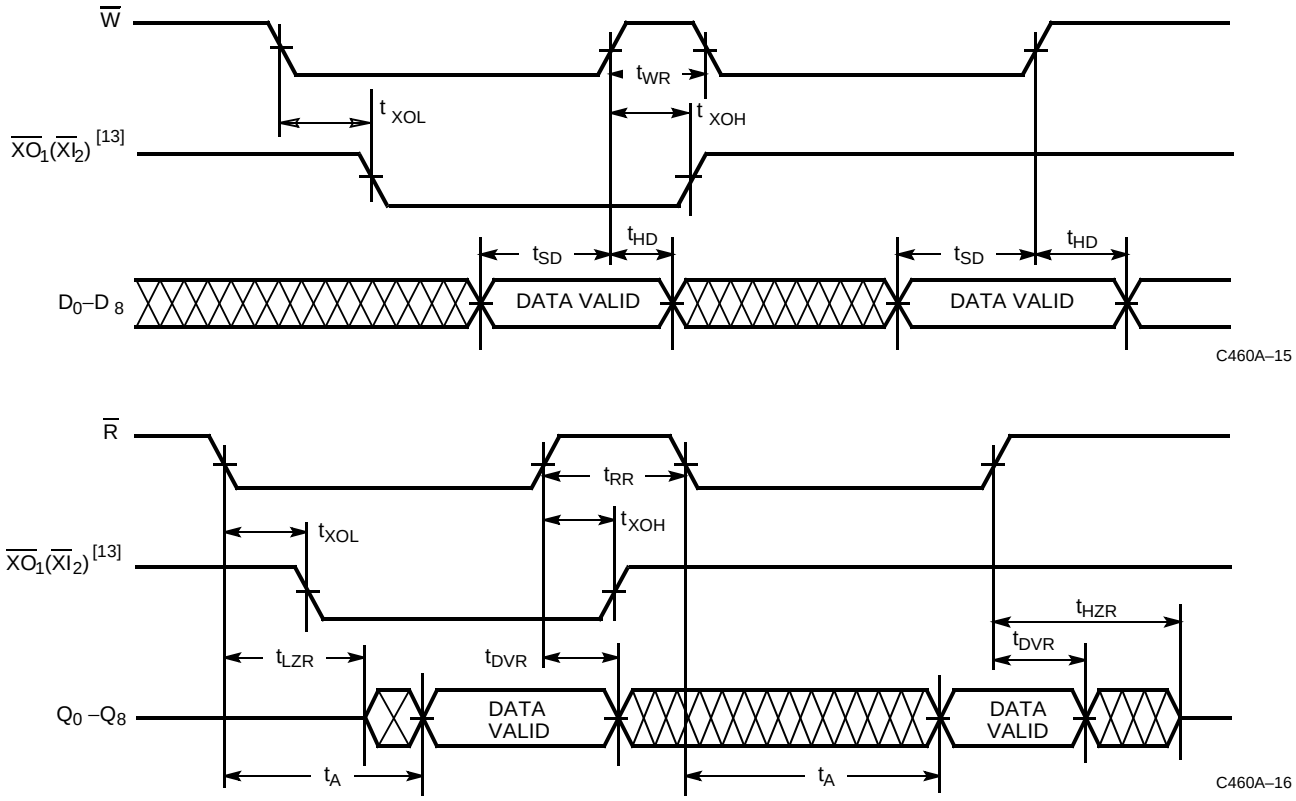
Empty Flag and Read Data Flow-Through Mode



C460A–14

Switching Waveforms[7] (continued)

Expansion Timing Diagrams



Note:
13. Expansion out of device 1 ($\overline{XO}_1$) is connected to expansion in of device 2 ($\overline{XI}_2$).

Architecture

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$), and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and Write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0–D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being half full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{RFF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0–Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a

number of writes equal-to-or-less-than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer incremented until equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding expansion in ($\overline{XI}$) and tying first load ($\overline{FL}$) to V_{CC} prior to a $\overline{MR}$ cycle. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (*see Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, expansion out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode, the first load ($\overline{FL}$) input, when grounded, indicates that this is the first part to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for Read and one is enabled for Write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created with word widths in increments of nine. When expanding in depth, a composite $\overline{FF}$ is created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

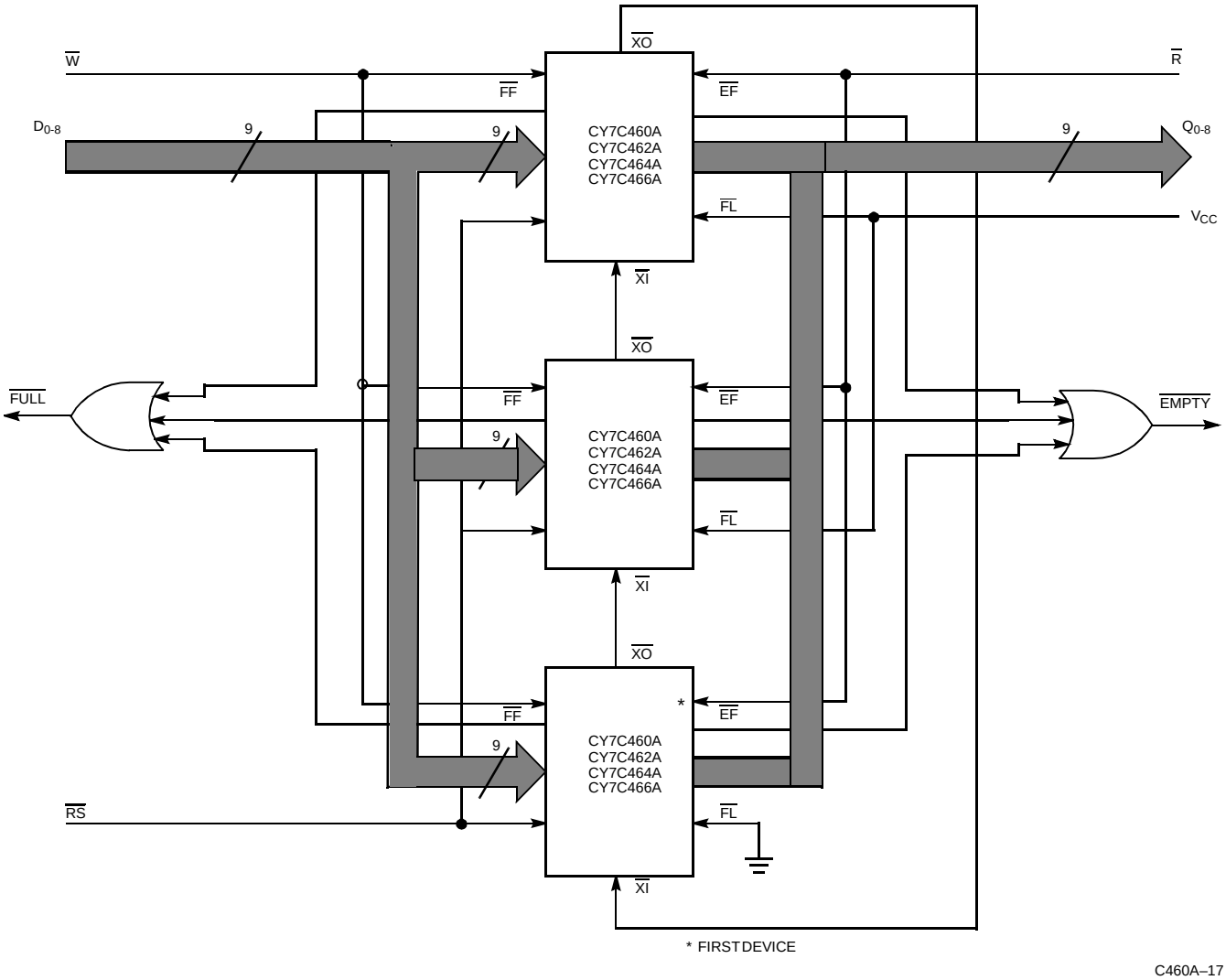


Figure 1. Depth Expansion

Ordering Information

8K x 9 Asynchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C460A-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460A-10PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460A-10PTC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C460A-10JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
15	CY7C460A-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460A-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460A-15PTC	P21	28-Lead (300-Mil) Molded DIP	
25	CY7C460A-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460A-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460A-25PTC	P21	28-Lead (300-Mil) Molded DIP	

16K x 9 Asynchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C462A-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462A-10PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462A-10PTC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C462A-10JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
15	CY7C462A-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462A-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462A-15PTC	P21	28-Lead (300-Mil) Molded DIP	
25	CY7C462A-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462A-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462A-25PTC	P21	28-Lead (300-Mil) Molded DIP	

32K x 9 Asynchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C464A-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464A-10PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464A-10PTC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C464A-10JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
15	CY7C464A-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464A-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464A-15PTC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C464A-15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
25	CY7C464A-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464A-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464A-25PTC	P21	28-Lead (300-Mil) Molded DIP	

Ordering Information (continued)

64K x 9 Asynchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C466A-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C466A-10PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C466A-10PTC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C466A-10JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
15	CY7C466A-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C466A-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C466A-15PTC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C466A-15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
25	CY7C466A-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C466A-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C466A-25PTC	P21	28-Lead (300-Mil) Molded DIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

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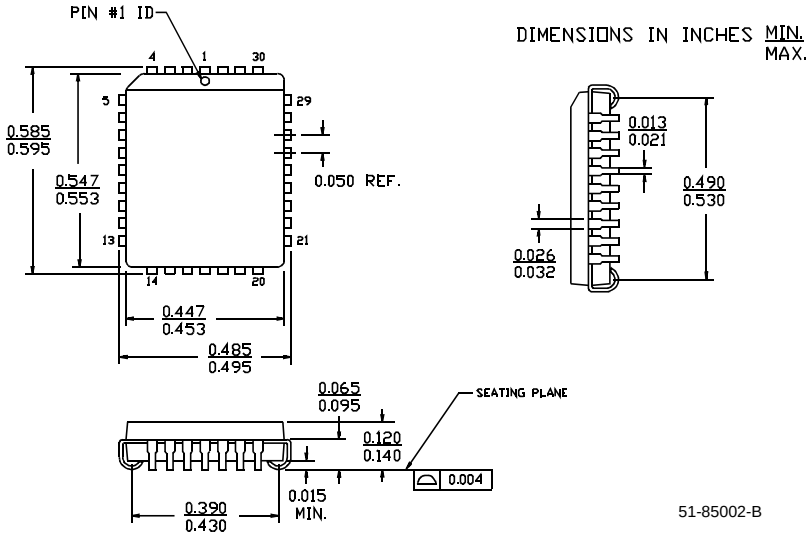
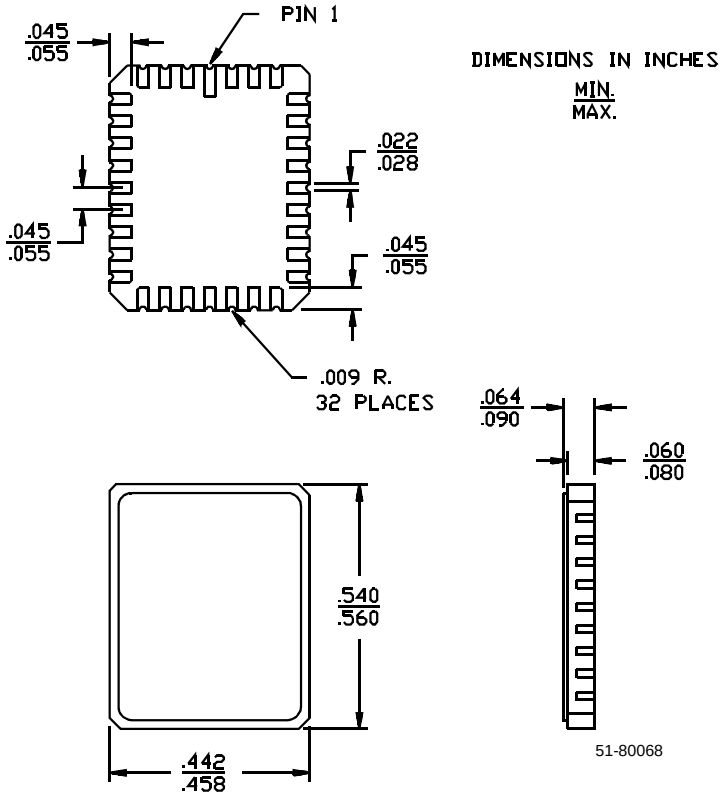
Package Diagrams

32-Lead Plastic Leaded Chip Carrier J65



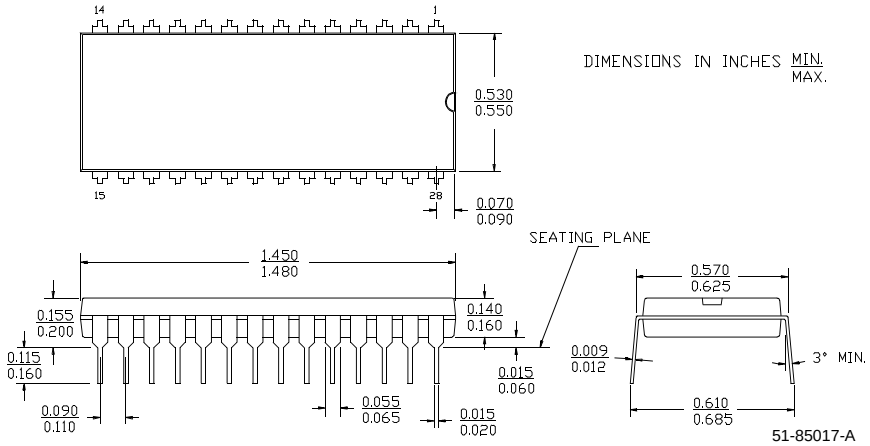
32-Pin Rectangular Leadless Chip Carrier L55

MIL-STD-1835 C-12

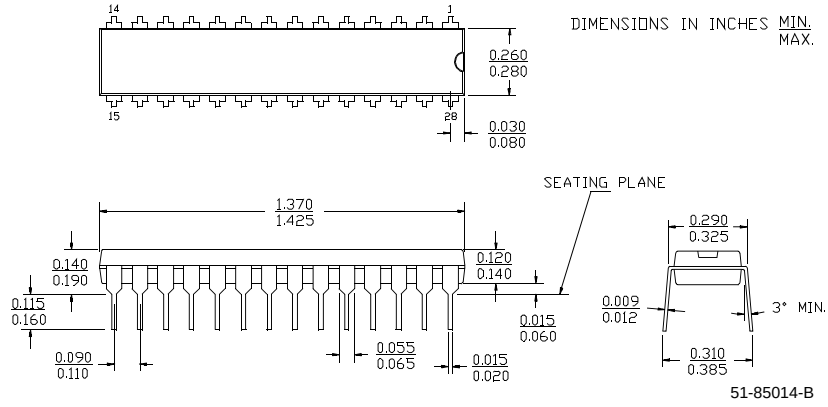


Package Diagrams (continued)

28-Lead (600-Mil) Molded DIP P15



28-Lead (300-Mil) Molded DIP P21



Document Title: CY7C460A, CY7C462A, CY7C646A, CY7C466A Asynchronous, Cascadable 8K/16K/32K/64K X 9 FIFOs Document Number: 38-06011				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106472	09/10/01	SZV	Change from Spec number 38-00627 to 38-06011
*A	122263	12/26/02	RBI	Power up requirements added to Maximum Ratings Information